

## CLAIMS

What is claimed is:

1. A multilayer circuit board comprising: a first layer (201); a fourth layer (204) substantially parallel to the first layer (201); a plurality of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd, 207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed; 311) formed within the first layer (201) of the multilayer circuit board and disposed in a first grid having, a first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) of the plurality of electrical contacts for routing within the first layer (201), and a second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) of the plurality of electrical contacts for routing within the fourth layer (204); and, a plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) formed between the first layer (201) and fourth layer (204) and each disposed adjacent at least one of the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) of the plurality of electrical contacts, the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd and 210cd; 310) having a spacing between each pair thereof larger than a smallest spacing between adjacent electrical contacts of the plurality of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd, 207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed; 311).

2. A multilayer circuit board according to claim 1, wherein the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) have a spacing of at least 1.1 times the first grid spacing.

3. A multilayer circuit board according to claim 2, wherein electrical contacts of the plurality of electrical contacts within the first grid alternate between the first subset of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) and the second subset of electrical contacts (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed).

4. A multilayer circuit board according to claim 1, wherein the first grid comprises a Cartesian grid comprising columns and rows, where each row and each column comprises alternating electrical contacts from the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) and the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed), the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) disposed in a second grid

comprising columns and rows having a substantially second pitch between adjacent vias, where electrical contacts for the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) are routed within the first layer (201) using one of a plurality of first electrical traces and electrical contacts for the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) are routed along the fourth layer (204) using one of a plurality of second electrical traces.

5. A multilayer circuit board according to claim 4, wherein pitch of the vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd and 210cd, 310) disposed in a second grid is at least 1.1 times larger than the pitch of the electrical contacts disposed in the first grid.

6. A multilayer circuit board according to claim 5, wherein pitch of the vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) disposed in a second grid is approximately the square root of two times larger than the pitch of the plurality of electrical contacts disposed in the first grid.

7. A multilayer circuit board according to claim 4, wherein the angle between the first grid and the second grid is approximately 45 degrees.

8. A multilayer circuit board according to claim 1, wherein the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) of the plurality of electrical contacts comprise bond pads.

9. A multilayer circuit board according to claim 1, wherein the vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) are disposed at opposite sides of adjacent electrical contacts belonging to the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed).

10. A multilayer circuit board according to claim 1, comprising a first substrate, where the first layer (201) is disposed within a first outside surface of the first substrate and where the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd and 210cd; 310) are drilled through the first substrate to a second other outside surface thereof, where the fourth layer (204) is disposed within the second other outside surface of the first substrate.

11. A multilayer circuit board according to claim 1, comprising a core layer disposed between the first and fourth layers, wherein the core layer comprises a plurality of other layers (202, 203) that are substantially parallel to the first layer (201) and the fourth layer (203) and the plurality of other layers (202, 203) comprising a plurality of non-

conducting areas (250) that surround the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310).

12. A multilayer circuit board according to claim 11, comprising an electrically conducting material (251) disposed about the plurality of non-conducting areas (250) for reducing a bi-planar cross-talk between the first layer (201) and the fourth layer (204).

13. A multilayer circuit board according to claim 12, wherein the plurality of non-conducting areas (250) are disposed in such a manner that vias formed on adjacent electrical contacts from the plurality of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd, 207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) are other than supported due to overlap between adjacent non-conducting areas (250).

14. A multilayer circuit board according to claim 13, wherein each of the plurality of non-conducting areas (250) is free of all other electrical contact other than a via (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) disposed therein once the multilayer circuit board is formed.

15. A multilayer circuit board according to claim 1, wherein each via (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) is adjacent at least two electrical contacts.

16. A method of manufacturing a multilayer circuit board comprising: providing a first layer (201); providing a fourth layer (204) substantially parallel to the first layer (201); disposing a plurality of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd, 207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed; 311) in a first grid within the first layer, the plurality of electrical contacts arranged in a first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) and a second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed); routing the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) of electrical contacts within the first layer (201); forming vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) between the first layer (201) and fourth layer (204), each via adjacent at least one of the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) of the plurality of electrical contacts and each via spaced from other vias by at least 1.2 times a minimum spacing between electrical contacts of the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) and the second subset (207ba, 207da,

207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed); and, routing the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) of the plurality of electrical contacts within the fourth layer (204).

17. A method according to claim 16, wherein the pitch between adjacent vias is approximately a square root of two times the pitch of the plurality of electrical contacts (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd, 207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed; 311).

18. A method according to claim 16, comprising: providing a first plurality of electrical traces disposed within the first layer (201) for routing of the first subset (207aa, 207ca, 207ea, 207bb, 207db, 207ac, 207cc, 207ec, 207bd, 207dd) of electrical contacts; and providing a second plurality of electrical traces disposed within the fourth layer for routing of the second subset (207ba, 207da, 207ab, 207cb, 207eb, 207bc, 207dc, 207ad, 207cd, 207ed) of electrical contacts, wherein a number of elements within the second plurality is within 50% of a number of elements of the first plurality.

19. A method according to claim 18, wherein a number of elements within the second plurality is within 10% of a number of elements of the first plurality.

20. A method according to claim 16, wherein the angle is approximately 45 degrees.

21. A method according to claim 16, comprising providing a core layer between the first layer (201) and the fourth layer (204), wherein the core layer comprises a plurality of other layers (202, 203) that are substantially parallel to the first layer (201) and the fourth layer (204), the plurality of other layers (202, 203) comprising a plurality of non-conducting areas (250) that surround the plurality of vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310).

22. A method according to claim 21, comprising providing an electrically conducting material (251) disposed about the plurality of non-conducting areas (250) for reducing a bi-planar cross-talk between the first layer (201) and the fourth layer (204).

23. A method according to claim 21, wherein the plurality of non-conducting areas (250) are disposed in such a manner that vias (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) formed on adjacent electrical contacts from the plurality of electrical contacts are other than supported due to an overlap between adjacent non-conducting areas.

24. A method according to claim 23, wherein each of the plurality of non-conducting areas (250) is free of all other electrical contact other than a via (210aa, 210ba, 210ab, 210bb, 210bc, 210ac, 210bc, 210ad, 210bd, 210cd; 310) disposed therein once the multilayer circuit board is formed.